

Influence of Thiol Self-Assembled Monolayer Processing on Bottom-Contact Thin-Film Transistors Based on n-Type Organic Semiconductors

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The performance of bottom-contact thin-film transistor (TFT) structures lags behind that of top-contact structures owing to the far greater contact resistance. The major sources of the contact resistance in bottom-contact TFTs are believed to reflect a combination of non-optimal semiconductor growth morphology on the metallic contact surface and the limited available charge injection area versus top-contact geometries. As a part of an effort to understand the sources of high charge injection barriers in n-channel TFTs, the influence of thiol metal contact treatment on the molecular-level structures of such interfaces is investigated using hexamethyldisilazane (HMDS)-treated SiO₂ gate dielectrics. The focus is on the self-assembled monolayer (SAM) contact surface treatment methods for bottom-contact TFTs based on two archetypal n-type semiconductors, α,ω -diperfluorohexylquaterthiophene (DFH-4T) and *N,N'*bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN₂). TFT performance can be greatly enhanced, to the level of the top contact device performance in terms of mobility, on/off ratio, and contact resistance. To analyze the molecular-level film structural changes arising from the contact surface treatment, surface morphologies are characterized by atomic force microscopy (AFM) and scanning tunneling microscopy (STM). The high-resolution STM images show that the growth orientation of the semiconductor molecules at the gold/SAM/semiconductor interface preserves the molecular long axis orientation along the substrate normal. As a result, the film microstructure is well-organized for charge transport in the interfacial region.

(RFID) tags, and organic chem- and bio-sensors.^[1–16] For these reasons, intensive research efforts are in progress at many universities, research institutes, and companies.^[17–37] Nevertheless, poor understanding of metal electrode–semiconductor interfacial phenomena is one of the critical obstacles limiting OTFT performance, optimization, and application.

There are several types of thin-film transistor (TFT) structures, which find application in various devices. They can be categorized first as either top-gate or bottom-gate structures (Figure 1).^[38] The top-gate structure (Figure 1C) is the most frequently used device geometry for complementary metal-oxide-semiconductor (CMOS) transistor fabrication^[39] and offers many advantages in conventional metal-oxide-semiconductor field-effect transistors. For example, using ion implantation methods, source-drain electrodes can be defined and the SiO₂ gate dielectric layer can be created using thermal growth. The only additional deposition layer required is the gate electrode, so top-gate device fabrication significantly reduces processing steps. On the contrary, typical amorphous Si TFTs

used for the fabrication of display backplanes are based on the bottom-gate architecture. In organic TFTs, top-gate structures enhance the air stability of the semiconductor layer by encapsulating it with the gate dielectric.^[40] However, this usually results in poor dielectric film morphology since it depends on the morphology of the underlying semiconductor film, which is usually considerably rougher than the Si/SiO₂ surface. In addition, unintentional doping of semiconductor films during dielectric deposition can erode the OTFT $I_{\text{on}}/I_{\text{off}}$ ratio.^[41] For these reasons, bottom-gate structures are more commonly used in OTFTs since all components are introduced separately in fabrication and therefore, the bottom-gate structure reduces the number of processing steps. A more important criterion in OTFT design is whether the device is bottom-contact or not, since only bottom-contact structures are compatible with conventional lithographic processing.

1. Introduction

Organic thin-film transistors (OTFTs) are key components for fabricating revolutionary organic electronic products such as flexible displays, organic radio frequency identification

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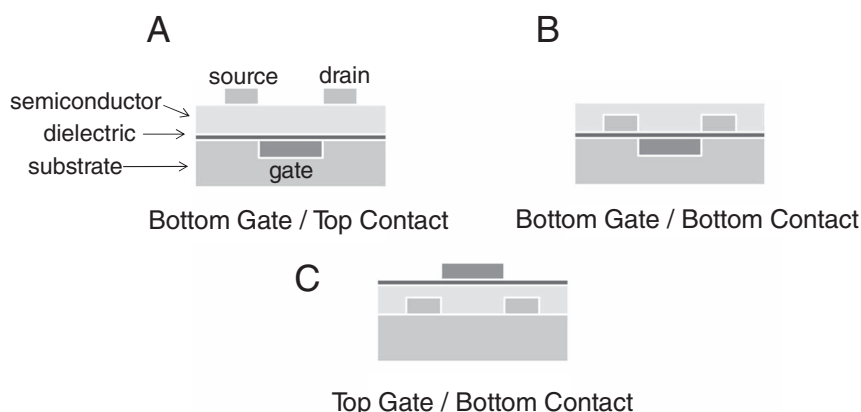


Figure 1. TFT device structures employed in this study.

Nevertheless, in terms of device performance, bottom-contact OTFT structures are generally far inferior to the top-contact structures. This is particularly true for n-channel TFTs where the contact resistance of the bottom-contact structure is greater than that in the top-contact geometries. This can be a very serious problem, especially as the device size is reduced. The measured total resistance is composed of the channel resistance and the contact resistance, with the channel resistance proportional to the channel length, and the contact resistance independent of channel length. In short channel devices, organic TFT performance is generally dominated by contact resistance rather than by gate-field-modulated channel resistance.^[42–48] Importantly, as the device size is scaled down, the speed of organic integrated circuits may not be limited by the intrinsic carrier mobility of the organic semiconductor, but rather by the contact resistance within the TFT. Therefore, any attempt at improving device structure design and fabrication processes intended to reduce contact resistance in organic TFTs is arguably as important as efforts directed at increasing the intrinsic organic semiconductor carrier mobility.

Several effects are believed to underlie the greater contact resistance observed in bottom-contact OTFT structures (Figure 1B). The first source is a discontinuous semiconductor film growth morphology over the interface between the SiO₂ channel region and the metal electrode.^[49] This is associated with random semiconductor molecular growth orientations, leading to high charge injection barriers at this interface. The second source arises from intrinsic differences in the semiconductor grain structure that grows on the dielectric surface versus that on the metal electrode surface. Larger grains are usually observed in the channel region rather than on the metal electrodes.^[49] This grain size disparity causes discontinuities in molecular ordering at the boundary line, which increases the charge injection barrier. The third source of contact resistance is the difference in the charge injection area size. In top contact structures (Figure 1A), the charge injection area consists of the entire pristine bottom surface of the electrodes.^[50] Therefore, the size of the charge injection area is relatively large. The injected charges form a 2D carrier gas at the organic semiconductor/dielectric interface since the electric field is induced by the gate voltage, meaning that charges are transported primarily along the interface between the semiconductor layer and the

dielectric.^[51] In contrast, the charge injection area is smaller and less pristine in the bottom-contact devices (Figure 1B). Since the electrodes are attached to the dielectric surface, the bottom surface of the electrode no longer plays a major role as the charge-injection area. As a result, the charge injection occurs predominantly from the small portion of the electrode side walls.

The most reliable technique devised to date to overcome the aforementioned disadvantages of the bottom-contact OTFT device structure is to treat the metal contact surface with a self-assembled monolayer (SAM)-forming reagent, such as a thiol for p-type organic semiconductors.^[52–58] If the surface of a gold electrode is coated with an

alkyl/aryl thiol SAM before organic semiconductor deposition, the dispersion in organic semiconductor grain size is substantially reduced and the overall grain size is increased to approximately that in the channel region.^[54] Indeed, chemically tailored source/drain contacts induce crystalline growth of p-type semiconductor films that can extend tens of millimeters into the transistor channel even for solution growth processes.^[53] In addition to this film morphology change, the effect on thiol SAM treatment of metal electrodes is also interpreted in terms of interfacial energy alignment. The organic SAMs modify the metal work function; in particular functional groups with dipole moments significantly alter the size of the work function.^[59–64] As a consequence, the charge injection barrier of the semiconductor-metal electrode interface can be decreased in favor of OTFT operation.

Another important OTFT surface treatment procedure is organosilane SAM growth on the hydroxylated surfaces of SiO₂ gate dielectrics. After organic semiconductor deposition on hydroxylated SiO₂ surfaces, the surface SiOH functional groups can play a major role as charge traps, which can significantly disrupt charge transport. By greatly decreasing the density of surface SiOH groups, organosilane SAM deposition suppresses carrier trapping.^[65,66] Furthermore, alkylsilane SAMs lower the surface energy, thus enhancing the crystallinity of the lipophilic semiconductor growth.^[67–70]

To date, efforts to improve OTFT bottom-contact device performance have focused on p-type semiconductor-based devices, and little work has been done to optimize bottom contacts to n-type materials.^[49–51,54] Here, we select *N,N'*bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN₂)^[71] and α,ω -diperfluorohexylquarterthiophene (DFH-4T)^[72,73] (Figure 2) as two distinctive examples of small-molecule n-type semiconductors. PDI-8CN₂ has a perylene core with two electron-withdrawing cyano groups, while DFH-4T features an oligothiophene backbone with perfluoroalkyl electron-withdrawing substituents. These materials exhibit unique properties in terms of OTFT performance, with PDI-8CN₂ being one of the most promising organic n-type semiconductors due to the high TFT mobility, low threshold voltage, and impressive air stability. The device performance of DFH-4T is somewhat less than that of PDI-8CN₂, however, it is a useful material for investigating molecular structure–device performance relationships since

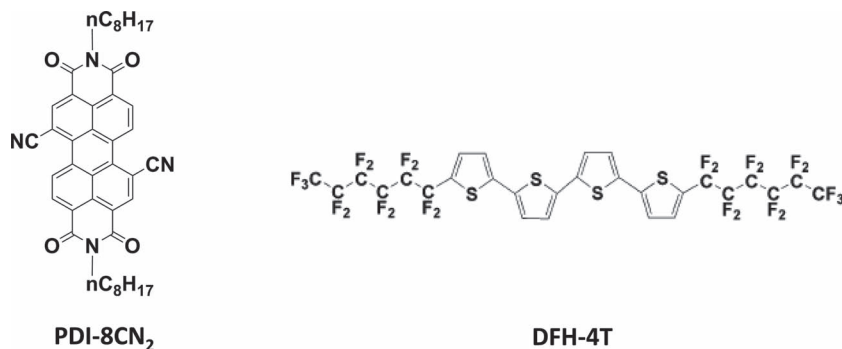


Figure 2. Semiconductors used in the present OTFT fabrication experiments.

it exhibits excellent n-type transport in top-contact TFTs, but poor charge transport in bottom-contact devices. We previously reported that the growth direction of DFH-4T molecules on gold surfaces is parallel to the substrate plane in the initial phases of film growth.^[74] However, after several molecular layers are deposited, the molecular growth orientation changes from parallel to perpendicular to the electrode surface. The explanation for this is that initially the adsorbate–substrate interactions are stronger than the adsorbate–adsorbate interactions and hence dominate the film growth process. However, at certain critical film coverage, the free energy of the substrate–adsorbate interaction is no longer greater than the adsorbate–adsorbate interaction. At this point, the growth mode switches from layer-by-layer to island growth. Due to this molecular alignment variation in the interfacial region, the charge injection from the gold electrode into the DFH-4T layer is significantly obstructed, introducing a high charge injection barrier. Therefore, an intriguing question is whether it is possible to enhance bottom-contact device performance in n-type OTFT systems using the surface treatment methods successful for p-type semiconductors and to understand the reasons for the observed changes in device response.

2. Results and Discussion

TFTs were fabricated in both bottom-gate–top-contact and bottom-gate–bottom-contact configurations (Figure 1). In both of the cases, highly doped p-type (100) silicon wafers ($<0.004 \, \Omega \, \text{cm}$) were used as gate electrodes as well as substrates, and 300 nm thermally grown SiO_2 on Si was used as the gate insulator. After hexamethyldisilazane (HMDS) deposition, the advancing aqueous contact angle on the surface was 95° . Next, organic semiconductor thin films (50 nm) were vapor-deposited onto the SiO_2/Si substrates held at a preset temperature of 80°C for DFH-4T and 110°C for PDI-8CN₂ with deposition rates of $0.3 \, \text{\AA} \, \text{s}^{-1}$ at 6×10^{-6} Torr, employing a high-vacuum deposition chamber. Next, 50 nm gold source and drain electrodes were vapor-deposited at 2×10^{-6} Torr through a shadow mask in a high-vacuum deposition chamber.

Devices were fabricated with typical channel lengths of 50, 100, 200, 300, 400, and 500 μm and with a channel width of 2000 μm . In the case of bottom-contact devices, gold electrodes were deposited before semiconductor film growth. Thiol treatment in ethanol solution immediately followed the gold deposition. For the thiol treatment process, three selected thiols, 4-chlorobenzenemethanethiol, 4-nitrobenzenethiol, and pentafluorothiophenol, (Figure 3) were deposited in 10 mM ethanol solution. To find the optimum surface treatment protocol, various combinations of the gold, thiol, and HMDS deposition procedures were examined in different

treatment sequences (Table 1).

Current–voltage (I – V) plots of OTFT performance were measured under vacuum, and transfer plots and output plots were recorded for each device. Key device performance parameters, such as carrier mobility (μ), threshold voltage (V_T), and on-off current ratio ($I_{\text{on}}/I_{\text{off}}$), were extracted from the source-drain current (I_{SD}) versus source-gate voltage (V_{SG}) characteristics employing standard data analysis procedures.^[39] Mobilities were obtained from the formula defined by the saturation regime in transfer plots, $\mu = 2I_{\text{SD}}L/[C_i W(V_{\text{SG}} - V_T)^2]$, where I_{SD} is the source-drain current, V_{SG} is the source-gate voltage, L is the channel length, W is the channel width, and C_i is the capacitance of the gate dielectric; threshold voltages were obtained from the \times intercepts of V_{SG} versus $I_{\text{SD}}^{1/2}$ plots, and contact resistances were calculated assuming a transmission line model, which is a model developed for amorphous silicon top-contact transistors.^[75,76] Contact resistances, R_c , were extracted from the $L = 0$ intersection of the measured device resistances, R , as a function of channel length. R values were obtained from the inverse slopes of the linear I – V curves in the output plot. The total resistance, R , can then be related to the channel length dependent resistance, R_{ch} , and a channel length independent contact resistance, R_c , that is associated with contacts, according to the transmission line method.^[75,76]

Aromatic thiol SAMs are known to have higher electrical conductance than alkyl thiol SAMs since the electrons are more delocalized in the π -electron rings.^[77,78] Among the three aromatic thiols selected^[50] (Figure 3), we find that

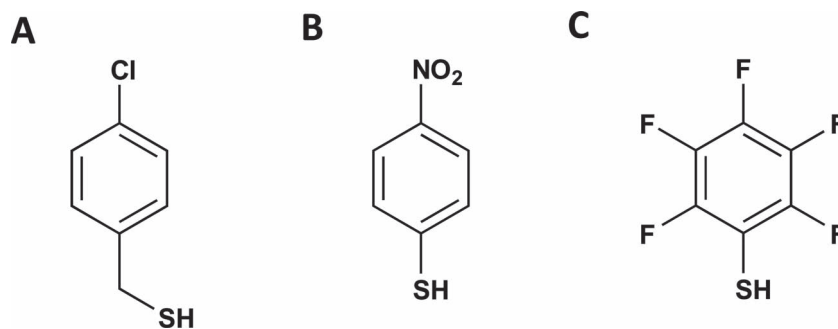
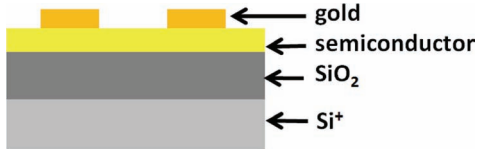
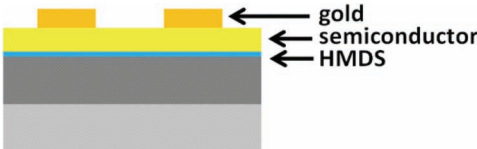
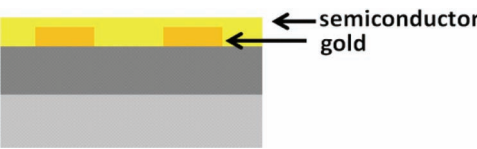
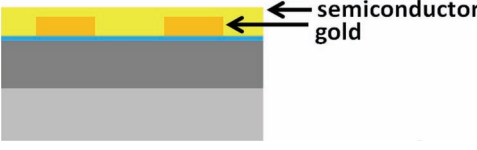
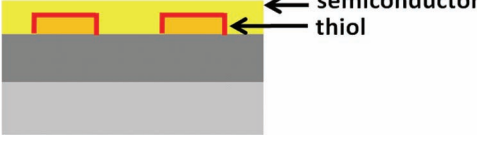
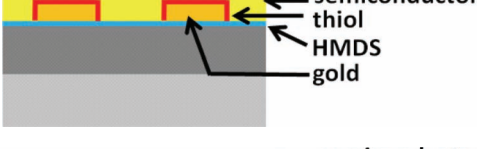
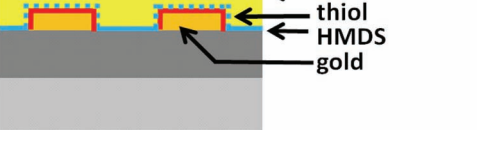
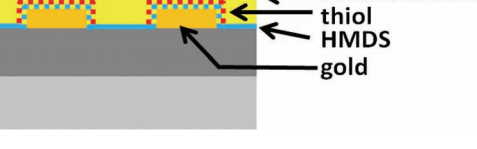
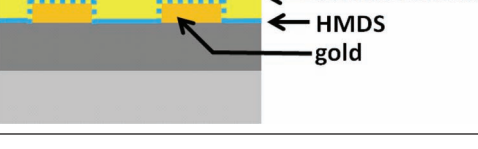


Figure 3. Aromatic thiols used in gold electrode treatment experiments. A) 4-chlorobenzenemethanethiol; B) 4-nitrobenzenethiol; and C) pentafluorothiophenol.

Table 1. Device types according to deposition order of component layers.

Device Type	Component Layers	Deposition Sequence
A		semiconductor/gold
B		HMDS/semiconductor/gold
C		gold/semiconductor
D		HMDS/gold/semiconductor
E		gold/thiol/semiconductor
F		HMDS/gold/thiol/semiconductor
G		gold/thiol/HMDS/semiconductor
H		gold/HMDS/thiol/semiconductor
K		gold/HMDS/semiconductor

Broken lines indicate partial SAM formation.

Table 2. Thiol treatment optimization for the DFH-4T OTFT system. Thiol A: 4-chlorobenzenemethanethiol, Thiol B: 4-nitrobenzenethiol, Thiol C: pentafluorothiophenol.

No.	Device Type	Structure	Substrate/ Dielectric	Deposition Order	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I_{on}/I_{off}	Contact Resistance [Ω cm]
1	A	Bottom-gate top-contact	Si/SiO ₂	DFH-4T/Gold	0.011 (±0.002)	64 ± 7	4.0 (±2.0)×10 ⁷	12 (±2)×10 ⁶ (V _g = 60 V) / 4 (±1)×10 ⁶ (V _g = 100 V)
2	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolA/ DFH-4T	0.029 (±0.012)	67.5 ± 11.1	2.1 (±3.4)×10 ⁶	1.6 (±0.6)×10 ⁶ (V _g = 60 V) / 6.2 (±1.7)×10 ⁵ (V _g = 100 V)
3	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolB/ DFH-4T	0.022 (±0.010)	66.3 ± 6.5	2.0 (±1.5)×10 ⁶	2.0 (±0.9)×10 ⁷ (V _g = 60 V) / 2.0 (±0.5)×10 ⁶ (V _g = 100 V)
4	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolC/ DFH-4T	0.033 (±0.013)	69.3 ± 6.4	1.6 (±2.1)×10 ⁶	2.4 (±1.2)×10 ⁷ (V _g = 60 V) / 1.1 (±0.4)×10 ⁶ (V _g = 100 V)

4-chlorobenzenemethanethiol-derived SAMs afford the best overall OTFT performance with the shortest deposition time (Table 2). For DFH-4T, 10 mM thiol solutions in anhydrous ethanol were employed with 70 min immersion times. However, since prolonged exposure to 4-chlorobenzenemethanethiol solutions severely delaminates the gold electrodes from the substrates, the substrates were immersed for only 1.0 min. When 4-nitrobenzenethiol and pentafluorothiophenol solutions are similarly applied for 1.0 min, device performance is found to be inferior to that of comparable devices treated with 4-chlorobenzenemethanethiol for 1.0 min. Overall, 4-chlorobenzenemethanethiol was found to be the most effective thiol for contact treatment because it yields similar or superior device performance with just 1.0 min deposition time.

In the case of PDI-8CN₂ OTFTs, 4-chlorobenzenemethanethiol was again found to afford the best device performance (Table 3). For the short thiol deposition times, it yields similar mobility and better I_{on}/I_{off} parameters than the other two thiols. In terms of threshold voltage, it is not more effective than pentafluorothiophenol. However, negative threshold voltages are frequently observed for pentafluorothiophenol-treated OTFT electrodes, meaning that the degree of unintentional doping of the semiconductor may be severe in these samples.^[72,73,79,80]

That 4-chlorobenzenemethanethiol SAM formation is rapid compared with the other thiols likely reflects the greater electron density at the sulfur atom in this thiol versus the other aromatic thiols. Since Cl has lower electron-withdrawing power than either F or NO₂ and the additional –CH₂ moiety insulates S electronically from the aromatic ring, the electron density at the sulfur atom of 4-chlorobenzenemethanethiol should be greater than in the two aromatic thiols. This greater electron density at S doubtless enhances the bonding to the gold electrode. The results of Liao et al.^[81] support this proposal. Here the effects of thiol substituents on chemisorption on gold surfaces were investigated by introducing five different functional groups (NO₂–, CF₃–, N(CH₃)₂–, CH₃–, CH₃S–) at the 4'-position of a series of mercaptobiphenyls. It was reported that CH₃S–Ph–Ph–SH undergoes adsorption most rapidly while NO₂–Ph–Ph–SH is the slowest. These results argue that increasing the electron-donating characters of the 4'-substituent accelerates the chemisorption process. As the substituent at the 4'-position becomes a stronger electron donor, the electron density at the SH group increases and the interaction strength with the gold surface is enhanced.

With regard to OTFT response, for DFH-4T transfer plots, the on-current values and the slopes of the source-drain current

Table 3. Thiol treatment optimization for the PDI-8CN₂ OTFT system. Thiol A: 4-chlorobenzenemethanethiol, Thiol B: 4-nitrobenzenethiol, Thiol C: pentafluorothiophenol.

No.	Device Type	Structure	Substrate/ Dielectric	Deposition Order	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I_{on}/I_{off}	Contact Resistance [Ω cm]
1	A	Bottom-gate top-contact	Si/SiO ₂	HMDS/ PDI-8CN ₂ / Gold	0.08 (±0.02)	5.35 (±3.03)	9.1 (±9.2)×10 ⁴	9.5 (±2.7)×10 ⁴ (V _g = 80 V) / 7.9 (±2.4)×10 ⁴ (V _g = 100 V)
2	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolA/ PDI-8CN ₂	0.10 (±0.02)	6.27 (±1.79)	1.5 (±2.3)×10 ⁵	4.1 (±0.8)×10 ⁴ (V _g = 80 V) / 3.2 (±0.5)×10 ⁴ (V _g = 100 V)
3	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolB/ PDI-8CN ₂	0.11 (±0.02)	4.65 (±1.13)	6.2 (±5.0)×10 ⁴	4.5 (±0.9)×10 ⁴ (V _g = 80 V) / 3.4 (±0.6)×10 ⁴ (V _g = 100 V)
4	F	Bottom-gate bottom- contact	Si/SiO ₂	HMDS/ Gold/ThiolC/ PDI-8CN ₂	0.11 (±0.02)	2.77 (±1.74)	1.3 (±1.6)×10 ⁴	4.0 (±0.7)×10 ⁴ (V _g = 80 V) / 3.2 (±0.8)×10 ⁴ (V _g = 100 V)

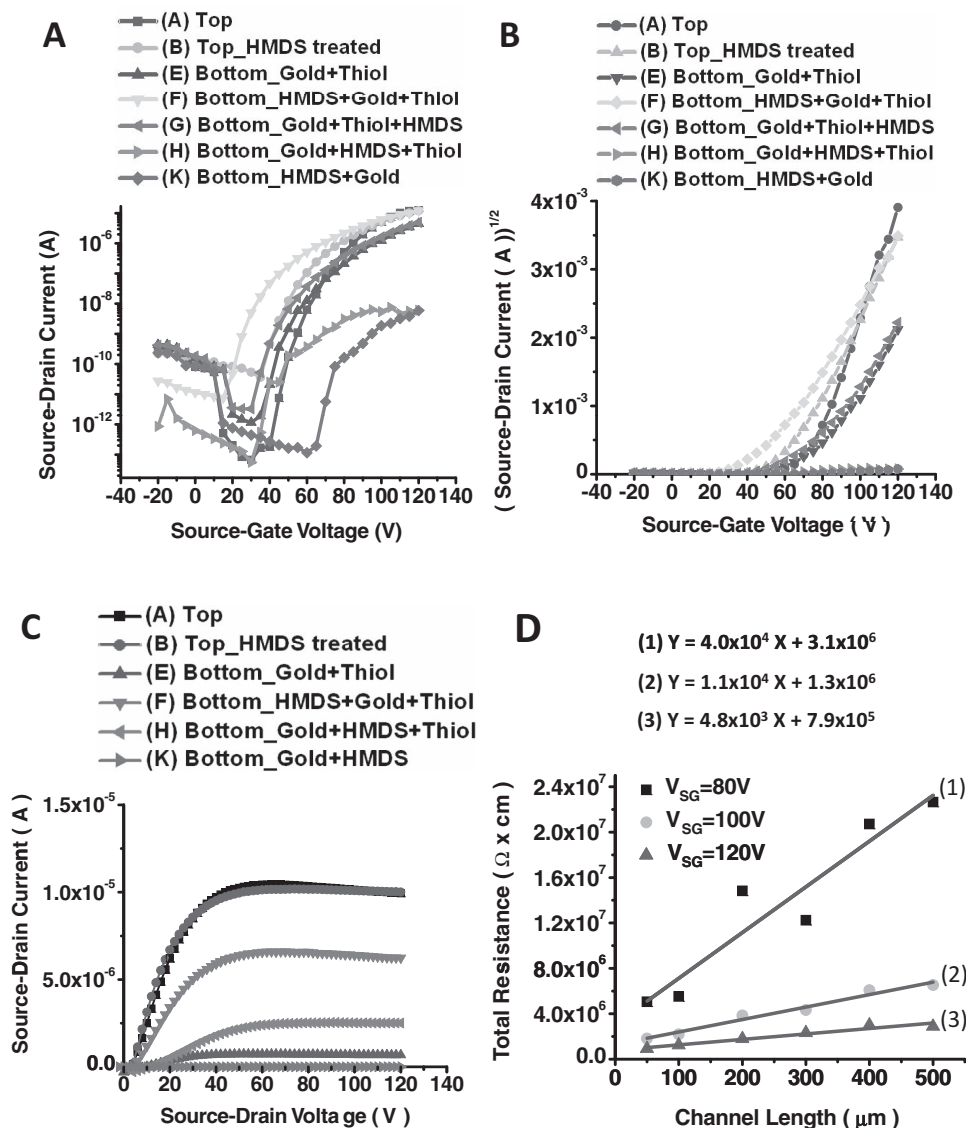


Figure 4. The effects of source, drain contact surface treatment in the DFH-4T OTFT system. A,B) Transfer plots (Channel length = 100 μm , Channel width = 2000 μm , $V_{\text{SD}} = 120\text{ V}$). C) Output plot (Channel length = 100 μm , Channel width = 2000 μm , $V_{\text{SG}} = 120\text{ V}$). D) Channel length vs. total resistance (Type F: Bottom-gate-bottom-contact/HMDS+Gold+Thiol, Channel width = 2000 μm). Since the resistance is inversely proportional to the channel width W , the total resistance R is normalized to R_W .

versus the source-gate voltage are substantially increased after thiol treatment of the bottom contacts (Figure 4A,B) and in the output plots a significant increase in on-current values is also observed (Figure 4C). To find the optimum surface treatment sequence that affords maximum device performance, a wide range of conditions was screened for the dielectric deposition and gold surface functionalization, and two deposition protocols, sequence F (HMDS + gold + thiol + DFH-4T) and sequence G (gold + thiol + HMDS + DFH-4T), were identified as most effective. All of the extracted device parameters for each surface treatment sequence are compiled in the Table 4. The nature of the thiol treatment has a far larger effect on device performance variations than does the HMDS treatment of the SiO_2 surface. However, when the two surface functionalization

methods are used together in the proper deposition sequence, the bottom-contact devices produce superior performance to that of the analogous top-contact devices. The total resistance versus channel length plots reveal a large reduction in contact resistance in the optimized bottom-contact device structures (Figure 4D). Without thiol treatment, it is impossible to extract contact resistance data due to low on-current values in the output plots, meaning that the contact resistance is excessive. After thiol treatment, the contact resistance is invariably decreased to the $10^6\ \Omega\ \text{cm}$ range at a source-gate voltage of 80 V (Table 4). The effect of HMDS treatment is more obvious in the contact resistance comparisons although it is not as dramatic as the effect of thiol treatment. One order of magnitude difference in contact resistance is observed between type E and type F OTFT structures (Table 4).

In the case of PDI-8CN₂ OTFTs, the trend is generally the same as for the aforementioned DFH-4T devices. As a consequence of the thiol treatment, the slopes of the source-drain current versus source-gate voltage in the transfer plots and the current levels in the output plots are greatly increased to the degree that the bottom-contact device performance is then superior to that of the analogous top-contact devices (Figure 5A–C). How-

ever, the difference in device response between thiol-treated devices and untreated ones is smaller than in the DFH-4T system (Table 5). Even type C and D devices without thiol treatment exhibit acceptable device performance, although type F is still the optimum fabrication sequence to achieve high performance. We suspect these differences reflect, among other factors, the good intrinsic materials properties of PDI-8CN₂ as a semiconductor. Compared to thiol treatments, the effects of HMDS surface treatment on PDI-8CN₂ device performance are small. However, enhancements are still evident in terms of threshold voltage and $I_{\text{on}}/I_{\text{off}}$ parameters between type C and type D structures. The total resistance versus channel length plot reveals a large reduction in contact resistance in the optimized bottom-contact device structures (Figure 5D). With thiol

Table 4. Variation of DFH-4T OTFT device performance with electrode surface treatment. Thiol A: 4-chlorobenzenemethanethiol.

No.	Device Type	Structure	Substrate/ Dielectric	Deposition Order	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	<i>I</i> _{on} / <i>I</i> _{off}	Contact Resistance [Ω cm]
1	A	Bottom-gate top-contact	Si/SiO ₂	DFH-4T/Gold	6.0 (±1.4)×10 ⁻²	68 (±14)	3.5 (±4.0)×10 ⁷	3.9 (±1.1)×10 ⁵ (V _g = 80 V)/ 2.1 (±0.9)×10 ⁵ (V _g = 100 V)
2	B	Bottom-gate top-contact	Si/SiO ₂	HMDS/ DFH-4T/Gold	5.2 (±2.1)×10 ⁻²	68 (±6)	1.3 (±1.2)×10 ⁶	4.6 (±1.9)×10 ⁵ (V _g = 80 V)/ 1.3 (±0.7)×10 ⁵ (V _g = 100 V)
3	C	Bottom-gate bottom-contact	Si/SiO ₂	Gold/DFH-4T	1.0 (±3.5)×10 ⁻⁵	66 (±11)	7 (±25)×10 ³	Too high
4	D	Bottom-gate bottom-contact	Si/SiO ₂	HMDS/Gold/ DFH-4T	2.2 (±3.3)×10 ⁻⁴	84 (±10)	1.8 (±2.9)×10 ⁴	Too high
5	E	Bottom-gate bottom-contact	Si/SiO ₂	Gold/Thiol-A/ DFH-4T	2.3 (±0.5)×10 ⁻²	70 (±9)	8.5 (±11)×10 ⁶	3.2 (±1.2)×10 ⁷ (V _g = 80 V)/ 4.4 (±1.3)×10 ⁶ (V _g = 100 V)
6	F	Bottom-gate bottom-contact	Si/SiO ₂	HMDS/Gold/ Thiol-A/ DFH-4T	3.4 (±1.6)×10 ⁻²	62 (±7)	1.4 (±0.9)×10 ⁶	1.5 (±0.7)×10 ⁶ (V _g = 80 V)/ 4.4 (±0.6)×10 ⁵ (V _g = 100 V)
7	G	Bottom-gate bottom-contact	Si/SiO ₂	Gold/Thiol-A/ HMDS/ DFH-4T	3.5 (±1.6)×10 ⁻²	62 (±4)	1.2 (±3.1)×10 ⁷	6.2 (±0.6)×10 ⁶ (V _g = 80 V)/ 2.6 (±0.8)×10 ⁵ (V _g = 100 V)
8	H	Bottom-gate bottom-contact	Si/SiO ₂	Gold/HMDS/ Thiol-A/ DFH-4T	1.3 (±1.4)×10 ⁻⁴	63 (±17)	1.2 (±3.1)×10 ⁴	Too high
9	K	Bottom-gate bottom-contact	Si/SiO ₂	Gold/HMDS	No device property			

treatment, the contact resistance is decreased from 10⁵ Ω cm in type C devices to 10⁴ Ω cm in type E devices at a source-gate voltage of 80 V (Table 5). Again, the effects of HMDS treatment on the OTFT parameters are not as significant as those

resulting from thiol treatment. The contact resistance of type C and type D structures is almost identical, and only small reductions in contact resistance are observed between types E and F structures (Table 5).

Table 5. Variation of PDI-8CN₂ OTFT device performance with electrode surface treatment. Thiol A: 4-chlorobenzenemethanethiol

No.	Device Type	Structure	Substrate/ Dielectric	Deposition Order	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	<i>I</i> _{on} / <i>I</i> _{off}	Contact Resistance [Ω cm]
1	A	Bottom-gate top-contact	Si/SiO ₂	PDI-8CN ₂ /Gold	0.06 (±0.03)	4.3 (±5.6)	2.6 (±2.1)×10 ⁴	8.0 (±2.2)×10 ⁴ (V _g = 80 V)/ 6.8 (±2.3)×10 ⁴ (V _g = 100 V)
2	B	Bottom-gate top-contact	Si/SiO ₂	HMDS/PDI- 8CN ₂ /Gold	0.08 (±0.04)	14.3 (±12.4)	4.8 (±5.0)×10 ⁴	4.2 (±1.2)×10 ⁴ (V _g = 80 V)/ 3.5 (±0.7)×10 ⁴ (V _g = 100 V)
3	C	Bottom-gate bottom-contact	Si/SiO ₂	Gold/PDI-8CN ₂	0.05 (±0.02)	5.5 (±5.6)	9.0 (±5.4)×10 ²	1.3 (±0.7)×10 ⁵ (V _g = 80 V)/ 1.1 (±0.6)×10 ⁵ (V _g = 100 V)
4	D	Bottom-gate bottom-contact	Si/SiO ₂	HMDS/Gold/ PDI-8CN ₂	0.05 (±0.02)	1.6 (±1.1)	9.6 (±2.8)×10 ³	1.6 (±0.8)×10 ⁵ (V _g = 80 V)/ 1.4 (±0.5)×10 ⁵ (V _g = 100 V)
5	E	Bottom-gate bottom-contact	Si/SiO ₂	Gold/Thiol-A/ PDI-8CN ₂	0.09 (±0.03)	2.5 (±1.2)	1.0 (±1.1)×10 ⁴	6.3 (±1.6)×10 ⁴ (V _g = 80 V)/ 6.2 (±1.2)×10 ⁴ (V _g = 100 V)
6	F	Bottom-gate bottom-contact	Si/SiO ₂	HMDS/Gold/ Thiol-A/PDI- 8CN ₂	0.10 (±0.02)	10.6 (±7.7)	4.5 (±4.6)×10 ⁴	3.2 (±0.9)×10 ⁴ (V _g = 80 V)/ 3.1 (±0.6)×10 ⁴ (V _g = 100 V)
7	G	Bottom-gate bottom-contact	Si/SiO ₂	Gold/Thiol-A/ HMDS/PDI- 8CN ₂	0.06 (±0.02)	6.8 (±2.8)	2.1 (±1.9)×10 ³	1.6 (±0.8)×10 ⁵ (V _g = 80 V)/ 1.3 (±1.0)×10 ⁵ (V _g = 100 V)
8	H	Bottom-gate bottom-contact	Si/SiO ₂	Gold/HMDS/ Thiol-A/PDI- 8CN ₂	0.08 (±0.01)	9.8 (±5.4)	6.2 (±5.0)×10 ⁴	1.3 (±0.5)×10 ⁵ (V _g = 80 V)/ 1.0 (±0.6)×10 ⁵ (V _g = 100 V)
9	K	Bottom-gate bottom-contact	Si/SiO ₂	Gold/HMDS	0.01 (±0.01)	11.8 (±9.1)	1.0 (±1.3)×10 ³	6.3 (±3.3)×10 ⁵ (V _g = 80 V)/ 5.9 (±2.1)×10 ⁵ (V _g = 100 V)

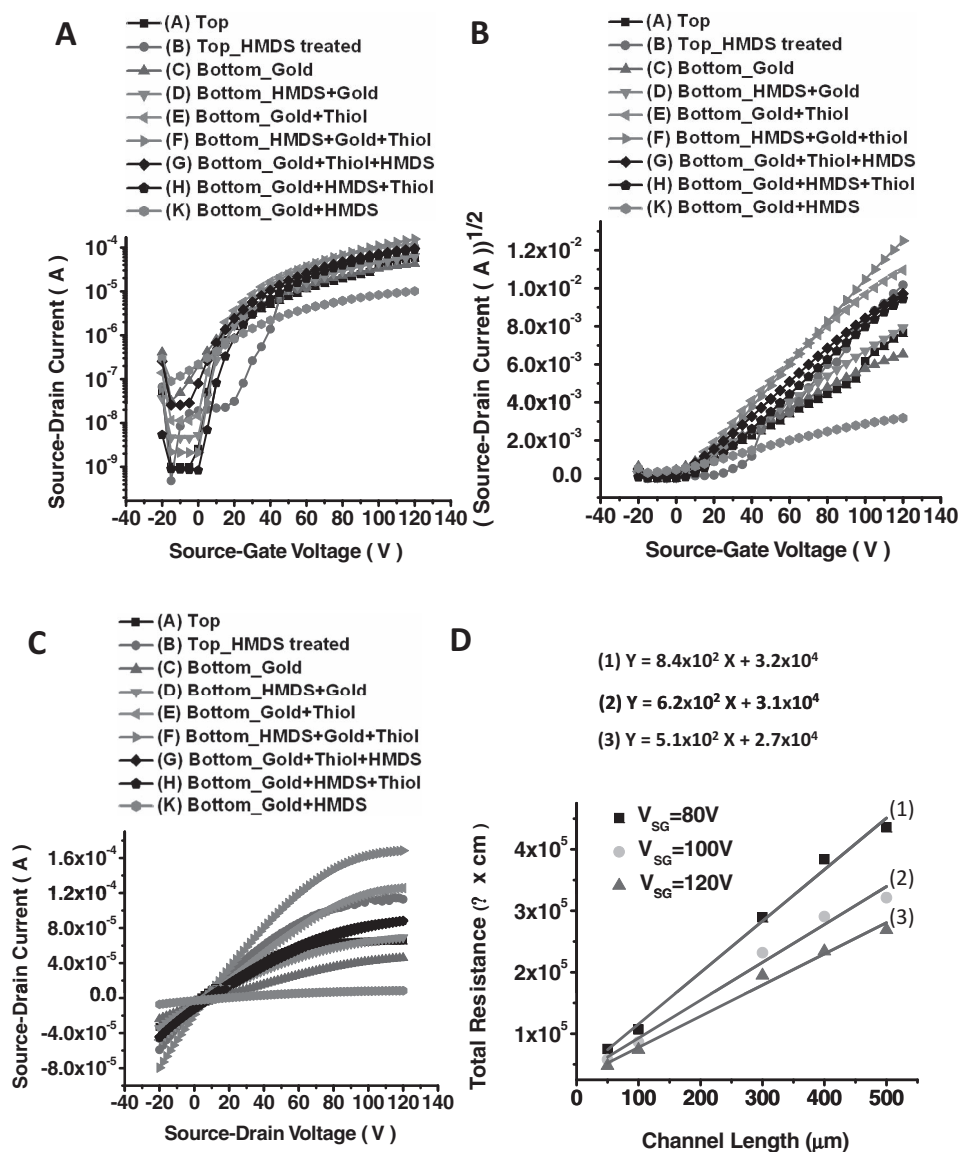


Figure 5. The effects of source, drain contact surface treatment in the PDI-8CN₂ OTFT system. A,B) Transfer plots (Channel length = 100 μm, Channel width = 2000 μm, V_{SD} = 100 V). C) Output plot (Channel length = 100 μm, Channel width = 2000 μm, V_{SG} = 120 V). D) Channel length vs. total resistance (Type F: Bottom-gate-bottom-contact/HMDS+Gold+Thiol, Channel width = 2000 μm). Since the resistance is inversely proportional to the channel width *W*, the total resistance *R* is normalized to *R_W*.

The channel length dependence of the TFT mobility dramatically illustrates the effects of thiol electrode treatment (Figure 6A,B). The apparent mobility of bottom-contact TFTs decreases as the channel length is decreased. This decrease in mobility presents a serious problem when high-performance devices with short channel lengths are fabricated. The low measured mobility of the short-channel bottom-contact TFTs is mainly due to high contact resistance in the bottom-contact configurations. Due to the effects of thiol treatment, the channel length dependence of the mobility in the bottom-contact devices is greatly reduced, to the magnitude of top-contact structures for both semiconductors.

As can be seen from the present discussion, the contact resistance decreases with increasing source-gate voltage due

to the increased carrier density in the channel and near the contacts (Figure 7A,B). Furthermore, in the case of bottom contacts, it can be seen that the contact resistance is less dependent on gate voltage than in top-contact devices. Due to this effect, bottom-contact devices in the PDI-8CN₂ system exhibit much less contact resistance in low-voltage operation (Figure 7B). Even in DFH-4T devices, the bottom-contact resistance is nearly comparable to the corresponding top-contact parameter at gate voltages lower than 60 V if we extrapolate the plots (Figure 7A). These results are consistent with the literature for p-type organic semiconductors.^[42,45,46] For example, Necliudov et al.^[46] measured the contact resistance of top- and bottom-contact pentacene OTFTs with Pd electrodes. They observed that the contact resistance of the top-contact devices sharply increases to even higher values than that of the corresponding bottom-contact counterparts at gate voltages less than -20 V. These results suggest the bottom-contact device is actually a better candidate for low power consumption device applications.

One interesting phenomenon to be explained is the high threshold voltages of DFH-4T devices. In OTFTs, the threshold voltage strongly depends on the density and energy of charge traps at the semiconductor/dielectric interface. The charge traps usually lie at a lower energy than the frontier molecular orbital energies of the semiconductor (the lowest unoccupied molecular orbital (LUMO) for *n*-channel semiconductors), and they must be completely filled with charge carriers before injection into the semiconductor layer. The energy difference between the source electrode work function and frontier molecular orbitals of the semiconductor (LUMO for *n*-channel semiconductors) represents an energy barrier opposing electron injection from the metal to the organic semiconductor. This injection barrier plays a key role in determining the threshold voltage since higher injection barriers will require higher gate voltages, meaning higher threshold voltages, to tune the LUMO energy. The density of charge traps at the TFT semiconductor/dielectric interface,

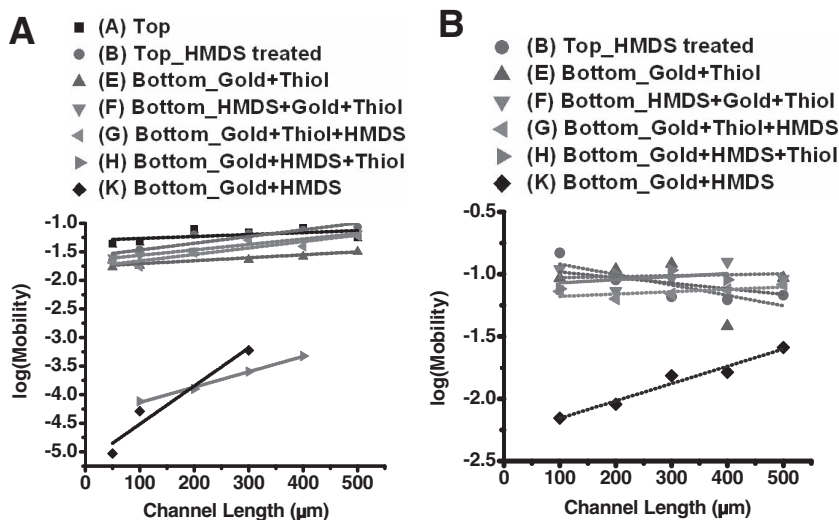


Figure 6. Channel length dependence of the field-effect mobility. A) DFH-4T OTFTs and B) PDI-8CN₂.

which are mainly caused by hydroxyl groups on the dielectric surface and ambient traps such as O₂ and H₂O, can be significantly reduced by HMDS treatment and by operating the devices under vacuum. In our study, we use HMDS-treated SiO₂ dielectrics for both DFH-4T and PDI-8CN₂ device fabrication and the devices are operated under vacuum. Therefore, the differences in threshold voltages between DFH-4T and PDI-8CN₂ devices are not due to hydroxyl groups on SiO₂ surface or ambient oxidants (O₂ and H₂O). Since the device fabrication and evaluation conditions are similar for the DFH-4T and PDI-8CN₂-based FETs, the differences in threshold voltages most likely reflect the differences between the LUMO energies of DFH-4T (−3.3 eV) and PDI-8CN₂ (−4.3 eV). The higher LUMO energy of DFH-4T makes these semiconductor thin films highly susceptible to semiconductor–dielectric surface traps with energies < −3.3 eV, whereas the charge carriers in thin films of PDI-8CN₂ are more stabilized in the relatively low-lying LUMOs against any trapping sites. On the other hand, the electron injection

barriers are estimated as ≈0.8 eV for PDI-8CN₂ and ≈1.8 eV for DFH-4T devices (the work function of gold electrode is taken as −5.10 eV). Thus, the noticeably larger electron injection barrier of DFH-4T contributes to the large threshold voltages in the DFH-4T-based devices, and this phenomenon has been reported many times before^[82,83] although a comprehensive theoretical study has not been established yet.^[84]

Another interesting observation in the present study is that device performance deteriorates when the HMDS is applied to the gold prior to thiol deposition in the case of DFH-4T system (Table 4). The reason is probably that HMDS treatment of the gold surface leaves residual materials which interfere with complete chemisorptive surface coverage by the SAM thiol. Although gold is generally known to have no stable surface oxides,^[85] King^[86] showed that oxidation of gold at room temperature can give a 17 Å thick Au₂O₃ layer, which is stable to extended exposure to ultrahigh vacuum and ethanol rinsing. This oxide layer apparently provides surface adhesion for the HMDS. Eventually, partially adsorbed HMDS molecules could play a role as contaminants in disturbing homogeneous thiol SAM coverage and would thus increase the resistance of the gold surface.^[87–89] To assess the level of contaminants on gold surface, X-ray photoelectron spectroscopy (XPS) measurements were conducted on the gold substrates and on the O₂ plasma cleaned gold substrates (Figure S1, Supporting Information). Carbon and oxide contaminants were observed on the surfaces, and the level of contamination is reduced after oxygen plasma cleaning (Figure S1A, S1B, Supporting Information). As a result, the amount of sulfur on the plasma-cleaned gold surfaces is greater than the amount on non-cleaned gold surfaces after thiol SAM formation (Figure S1C, Supporting Information). Although carbon contamination is a more serious problem for gold surfaces in general, Table S1 (Supporting Information) shows that the contamination itself does not affect the charge injection properties of the gold electrode/organic semiconductor interface in a major way. When DFH-4T devices are prepared without an HMDS SAM, O₂ plasma cleaning does not significantly affect the device performance. Therefore, the observed device performance deterioration after HMDS treatment is likely due to oxides since they are logical binding sites for HMDS molecules, and all the devices were fabricated on gold electrodes without O₂ plasma cleaning to protect the pre-deposited HMDS SAMs. The fact that device properties are marginal when only HMDS treatment is applied supports this speculation. Interestingly, this effect is not as obvious in the PDI-8CN₂ OTFT system (Table 5), however, the device performance is still lowest when HMDS treatment alone is applied to the gold electrodes.

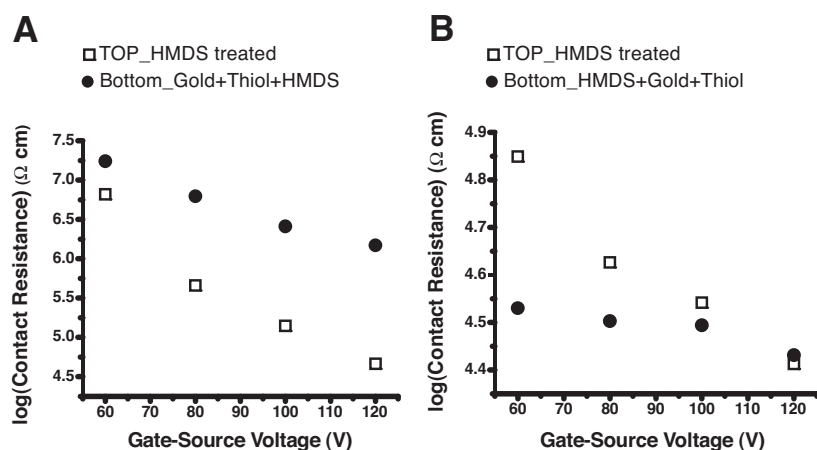


Figure 7. Gate voltage dependence of contact resistance. A) DFH-4T OTFTs and B) PDI-8CN₂.

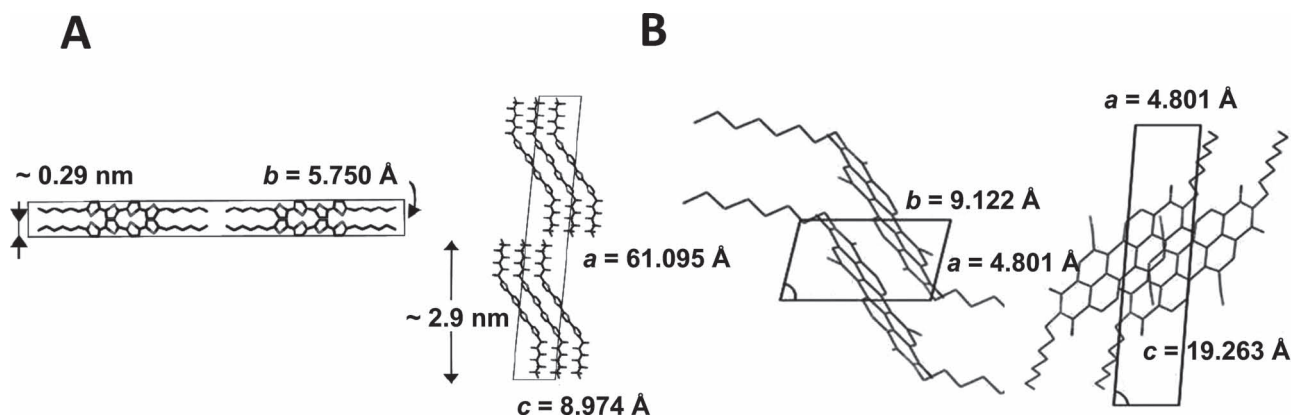


Figure 8. Crystal structures of DFH-4T (A)^[65,66] and PDI-8CN₂ (B).^[82]

Since we demonstrated here that contact surface optimization leads to substantial TFT performance enhancement for n-type semiconductors, the next step in understanding the origin of these effects is to investigate the microstructural changes in semiconductor growth due to these treatments. From AFM images (Figure S2, S3, Supporting Information), we observe qualitatively similar microstructural sources of contact resistance in the n-type bottom-contact devices as in p-type semiconductor systems.^[49–51] As might be expected, the grain sizes of the films on gold are much smaller than those of the films on the SiO₂ gate dielectric and this is plausibly one of the major sources of contact resistance. Furthermore, the boundary regions of the gold electrodes evidence irregular film structures, which are believed to interfere with charge transport.^[49] Nevertheless, we are unable to discern a significant grain size increase on the thiol-treated gold surfaces compared with the grain sizes on untreated gold surfaces, in contrast to what has been reported for p-type semiconductor systems.

If the bulk surface morphologies are similar, the key factors defining device performance differences may involve variations in interface microstructure. To investigate possible differences in molecular level interfacial microstructure, flame-annealed gold surfaces were introduced as the substrates since they expose homogeneous atomically flat Au(111) planes.^[90] The nanostructure was investigated using scanning tunneling microscopy (STM). Table S2 (Supporting Information) shows the film configurations investigated. Gold is the material of choice for device contacts, hence the STM study should elucidate film formation on contacts, especially for bottom contact devices. Since the thickness of 1 to 2 molecular monolayers is only 3 nm, the initial DFH-4T growth mode morphology can be observed in these thin films, while the 9 nm films detail the multilayer film morphology. According to the crystal structure of DFH-4T (Figure 8A), the unit cell has a 3 nm long axis and a 0.3 nm short axis. By analyzing the step heights of the surface morphology line profiles and comparing them with the length of crystal unit axes, the predominant growth mode and the orientation of the DFH-4T molecules can be determined.

Figure 9 shows a series of STM images of DFH-4T films performed at the nanoscale. Thus, Figure 9A,B compare the nanostructure of a 3 nm thick DFH-4T film deposited on bare and thiol-passivated Au(111) surfaces, over a 500 nm × 500 nm

scan area. The two films exhibit remarkably different nanostructures. The 3 nm DFH-4T layer deposited on bare Au(111) is amorphous and featureless. This organic monolayer completely wets the gold surface, exhibiting a nanostructure similar to that of typical self-assembled alkylthiol monolayers^[90,91] The underlying Au(111) planes are clearly evident. In marked contrast, the 3 nm DFH-4T film grown on thiol-treated Au(111) exhibits a granular morphology with a number of large flat grains approximately 100–200 nm in diameter. In some areas, the grains form overlapping terraces approximately 100 nm in width. Figure 9C,D compare the nanostructures of the 9 nm thick DFH-4T film on bare and thiol-passivated Au(111) surfaces respectively, also over comparable 500 nm × 500 nm scan areas. These two films also exhibit important differences in growth pattern, although in comparison to the 3 nm films, their morphological differences are not as pronounced. On both the unpassivated Au(111) and the passivated Au(111), 9 nm DFH-4T films exhibit a terraced morphology. In the unpassivated film, the grains show a distinct circular 3D vertical grain growth pattern arranged in islands. The grains are 70–170 nm in diameter, with the exposed terraces being approximately 20–40 nm in width. The passivated 9 nm film, on the other hand, exhibits large flat overlapping terraces with terrace widths of ≈30–120 nm. Circular island grain growth morphology is not observed in this film. The key difference between the 3 nm and the 9 nm thiol-passivated substrate films is in the arrangement of the flat grains, with the former showing a primarily granular growth while the latter exhibits an overlaid terraced growth pattern.

The absence of features such as terraces or grains in the monolayer thick 3 nm DFH-4T film on bare Au(111) indicates that the adsorbed molecules lie flat on the gold substrate. This orientation is favored by the energetics of the DFH-4T molecule-gold interaction in the first monolayer, which is greater than the molecule–molecule interaction present in vertically oriented DFH-4T molecules, observed in the subsequent multilayers^[74] (Figure 9A). The amorphous monolayer on gold and its poor molecular packing doubtless leads to suboptimal charge injection across the interface and the high contact resistance observed in bottom-contact devices. Upon thiol passivation of the Au(111) surface, the thiol SAM, in this case 4-chlorobenzenemethanethiol, wets the gold surface and quenches its high

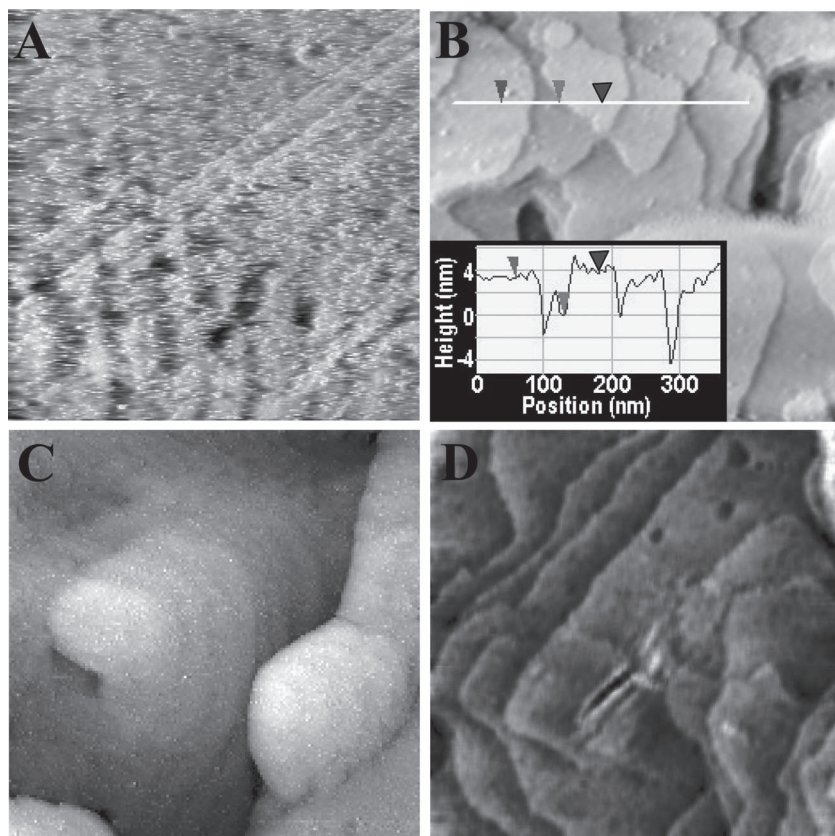


Figure 9. Dynamics of DFH-4T growth during monolayer to multilayer evolution on bare and thiol passivated Au(111). All STM images are taken over a 500 nm × 500 nm scan area. A) 3 nm DFH-4T on bare Au(111). B) 3 nm film of DFH-4T on thiol SAM/Au(111) substrate. C) 9 nm DFH-4T on bare Au(111) substrate. D) 9 nm DFH-4T on thiol SAM/Au(111) substrate. The inset in (B) shows a line profile, pinpointing two different grains each with a step height of 3 nm (unit cell *a*-axis of DFH-4T crystal structure), indicating that the molecule is oriented vertically on the substrate.

surface energy. The dynamics of the film growth are now governed by the stereochemistry and intermolecular interactions of the DFH-4T oligomers. Accordingly, subsequent deposition of DFH-4T on the thiol film leads to vertical alignment of the DFH-4T molecules, even in the first monolayer (Figure 9B). This is also clear from the line profile of the grain heights shown as the inset in Figure 9B. The arrows in the image and profile pinpoint the step heights for two grains. The measured step height of 3 nm corresponds to the long *a*-axis unit cell of the DFH-4T molecule (Figure 8A). The presence of large grains in the 3 nm DFH-4T film on thiol treated Au (111) seen in Figure 9B and the marked difference in the nanostructure in comparison to the amorphous and featureless 3 nm DFH-4T film/Au(111) seen in Figure 9A indicates that with the quenching of the substrate–molecule interactions by the thiol head group driven SAM formation, the dynamics of the subsequent film growth are now governed by the stereochemistry and intermolecular interactions of the DFH-4T oligomers. The evolution of the ordered grains into larger terraced domains progresses with increasing thickness of the organic film, as seen in the image of the 9 nm film shown in Figure 9D. Furthermore, the thiol treatment appears to ensure the growth of large grains even at greater thickness.

Considering the fact that there is little difference in the 50 nm DFH-4T film morphologies, this grain size difference appears to be alleviated as the orientation of molecules on bare gold surface changes from a planar geometry to a more upright configuration with increasing film thickness. This molecular orientation change of DFH-4T oligomers is shown schematically in Figure 10.

In the case of PDI-8CN₂ films, the effect of thiol passivation is less obvious relative to DFH-4T films. Submonolayers of PDI-8CN₂ films on a thiol-treated gold surfaces exhibit about 1.4 nm grain heights (Figure S4B, Supporting Information), just slightly greater than the 1.1 nm on bare gold (Figure S4A, Supporting Information). To have a direct comparison with DFH-4T, we obtained for the first time the crystal structure of PDI-8CN₂ (Figure 8B).^[92] From the crystal structure it is clear that the molecules cannot be lying completely flat even on the bare gold surface. This is considerably different from the flat molecular orientation of DFH-4T on gold. It is reasonable that this difference originates from differences in the molecular structures of the two molecules. Sulfur compounds are well known to strongly interact with gold surfaces. Accordingly, S atoms incorporated in DFH-4T molecules amplify molecular interactions with the gold surface. Specifically, the electron-deficient nature of DFH-4T facilitates charge transfer between low-lying DFH-4T π^* orbitals^[93] and the filled metal *d* band.^[94] If electron transfer to DFH-4T π^* orbitals is sufficiently large, ring-opening processes may occur, resulting

in the formation of thiolate species^[95] chemically bound to the gold surface. The lack of S atoms in the PDI-8CN₂ molecules rules out the possibility of this chemisorption pathway and argues that a weaker physisorption process dominates on gold. En route, PDI-8CN₂ molecules stand up to a certain degree without thiol passivation of gold surface. Furthermore, this explains why the differences in bottom contact PDI-8CN₂ device performance using thiol-treated contacts or non-treated contacts are relatively small compared with bottom contact DFH-4T devices (Table 4, 5). After 3 to 4 layers of molecules are deposited, the grain heights are increased up to 1.8 nm on both the bare gold surface and the thiol-treated gold surface (Figure S4C, S4D, Supporting Information). Given that this height is approximately the same as the length of the PDI-8CN₂ unit cell long molecular axis, the molecules are considered to be in fully standing up positions at this stage of the film growth.

The present STM studies show conclusively that thiol treatment acts as a wetting layer on the gold surface and reduces the high surface energy for subsequent semiconductor film growth. With the competing interaction from gold surface–molecular adlayer energetically quenched, the orientation of the molecules on the substrate is increasingly dictated by stereochemistry

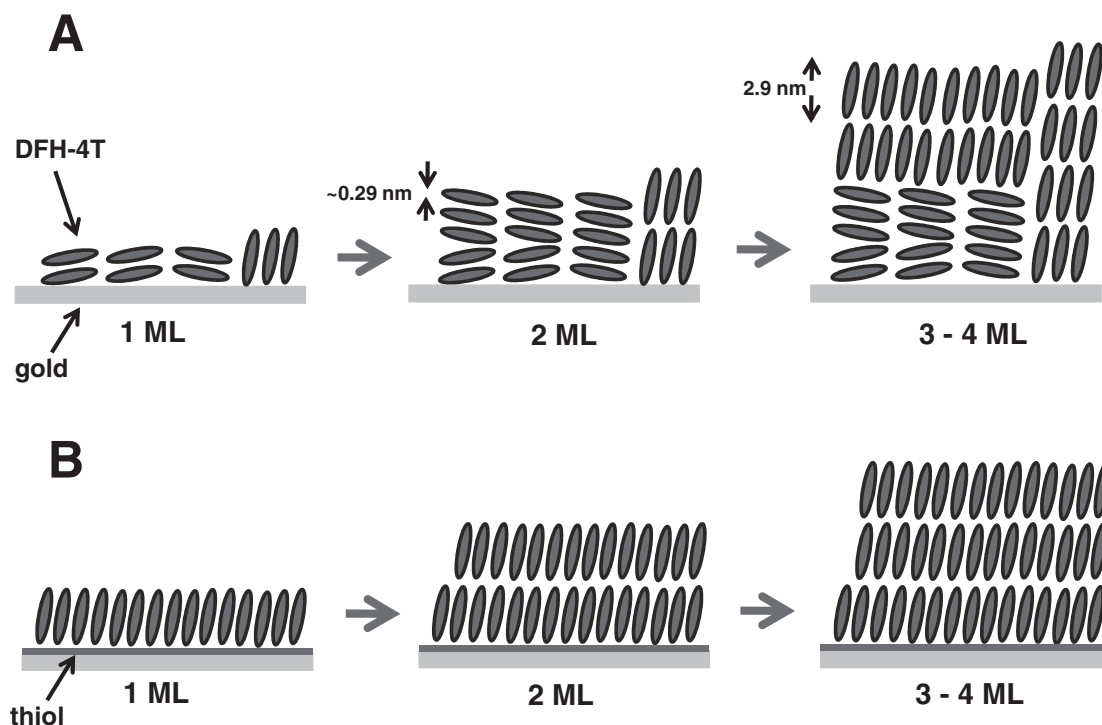


Figure 10. Proposed film structure at the organic semiconductor/gold electrode interface. A) On bare gold surfaces and B) on thiol-treated gold surfaces.

and intermolecular van der Waals interactions, as long as other parameters such as substrate temperature and deposition rate remain constant. Thus, in the subsequent multilayers, the film growth transitions from a layer-by-layer to a Stranski–Krastanov type growth,^[96] with the grains having large, smooth, and planar nanostructures. Such substrate–adsorbate interactions leading to different oligomer orientations with increasing film thickness are observed for various other types of substrates such as mica and graphite^[97] and for various types of molecules,^[98,99] the difference here being that we observe this switching in the very first monolayer upon thiol treatment. The orientation of the oligomers in the multilayers is shown schematically in Figure 10B. The adjacent stacking of the thiophene cores in these vertically oriented DFH-4T films leads to significant overlap of the core electrons and enhanced π – π interaction, leading to lowered charge injection barriers and more efficient OFET transport.

3. Conclusions

In summary, in an effort to address the contact surface wetting issues that lead to high charge injection barriers for n-channel bottom-contact OTFTs, thiol treatment of electrode surface was introduced prior to the deposition of the active semiconductors. We show that thiol treatment of gold electrode surfaces can dramatically enhance the device performance of bottom-contact n-type OTFT devices to exceed that of the corresponding top-contact devices. High-resolution STM images of the semiconductor films on thiol-treated and non-treated gold surfaces shows that thiol SAM formation promotes a standing-up growth

mode of the n-type semiconductor films in the metal–semiconductor interface region. With this study an understanding of organic multilayer growth dynamics on treated metallic surfaces begins to emerge. This understanding should eventually lead to true epitaxial organic film growth.

4. Experimental Section

Materials: The two n-type organic semiconductors, DFH-4T and PDI-8CN₂, were synthesized and purified as described elsewhere.^[71–73]

Device Processing: TFTs were fabricated in bottom-gate–top-contact and bottom-gate–bottom-contact configurations. In both of the cases, highly doped p-type (100) silicon wafers ($\rho < 0.004 \Omega \text{ cm}$) were used as gate electrodes as well as substrates and 300 nm SiO₂ thermally grown on Si was used as the gate insulator. The unit area capacitance (C_i) of the dielectric was 10 nF cm^{-2} . The substrate surface was treated with hexamethyldisilazane (HMDS) purchased from Sigma-Aldrich Chemical Co. A few drops of HMDS were loaded inside a glass self-assembly chamber under an N₂ blanket. The Si/SiO₂ substrates were then exposed to this atmosphere for at least 7.0 days to produce a hydrophobic surface. After HMDS deposition, the advancing aqueous contact angle was 95° . Organic semiconductor thin films (50 nm) were next vapor-deposited onto the Si/SiO₂ substrates held at previously optimized temperatures of 80°C for DFH-4T and 110°C for PDI-8CN₂, with a deposition rate of 0.3 \AA s^{-1} at 6×10^{-6} Torr, employing a high-vacuum deposition chamber (Denton Vacuum, Inc., USA). Gold source and drain electrodes (50 nm) were vapor-deposited at 2×10^{-6} Torr through a shadow mask in the vacuum deposition chamber. Devices were fabricated with typical channel lengths of 50, 100, 200, 300, 400, and 500 μm , with a channel width of 2000 μm . In the case of bottom-contact devices, gold electrodes were deposited before semiconductor film growth. Thiol treatment in ethanol solution followed gold deposition. For

thiol treatment, the three types of thiols, 4-chlorobenzenemethanethiol, 4-nitrobenzenethiol, and perfluorobenzenethiol were used as 10 mM thiol solutions with anhydrous ethanol (Sigma-Aldrich, >99%). For each thiol solution, the substrate was dipped for either 1 min or 70 min. To determine the optimum surface treatment method, various sequences and combinations of gold, thiol, and HMDS exposure were investigated using the different treatment sequences summarized in Table 1.

OTFT Characterization: I - V plots of device performance were measured under vacuum and transfer and output plots were recorded for each device. The I - V characteristics of the devices were measured using a Keithley 6430 subfemtoammeter and a Keithly 2400 source meter, operated by a local LabVIEW program and GPIB communication. Key device parameters, such as μ and I_{on}/I_{off} , were extracted from the I_{SD} versus V_{SG} characteristics employing standard procedures.^[39] Mobilities were obtained from the formula defined by the saturation regime in transfer plots, $\mu = 2I_{SD}L/[C_i W(V_{SG} - V_T)^2]$. Threshold voltage was obtained from x intercept of V_{SG} versus $I_{SD}^{1/2}$ plots and contact resistance was calculated based on the assumptions of the transmission line method, a model developed for amorphous silicon top contact transistors.^[75,76] R_c was obtained from the $L = 0$ intersection of the measured device resistance, R , as a function of channel length. R was obtained from the inverse slope of the linear I - V curves in the output plot. The total resistance, R , can be related to R_{ch} and R_c , which is associated with contacts, according to transmission line description.

Film Characterization: The organic films were deposited on flame-annealed Au(111)/mica surfaces. Chemical passivation of the Au(111) films was achieved by immersing the Au(111) films in a 10 mM ethanol solution of 4-chlorobenzenemethanethiol for an immersion time of 1 min. DFH-4T was subsequently deposited on the thiol-treated film. The DFH-4T deposition on the unpassivated Au(111) has been described previously.^[90] AFM measurements were performed using a JEOL-Microscope (JEOL Ltd. Japan) and Dimension Icon Scanning Probe Microscope (Veeco, USA) in the tapping mode. STM (Oxford Instruments) measurements were performed in vacuum using cut Pt/Ir tips, with the bias voltage applied to the sample. Topographic images were obtained in the constant current mode with a bias of 1.0 V and a typical set point tunnel current of 10–100 pA, which ensures a large tunnel junction impedance of 100–10 G, thereby avoiding destructive tip-surface interactions. XPS was conducted utilizing an Omnicron ESCA Probe system at ultra high vacuum ($\approx 10^{-10}$ mbar), with a monochromated Al K α X-ray source (1486 eV).

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